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<u>IN THE UNITED STATES PATENT AND TRADEMARK OFFICE</u>

Applicant:

Wendell P. Noble Jr. et al.

Examiner:

Jack Chen

Serial No.:

09/866938

Group Art Unit:

2813

Filed:

May 29, 2001

Docket:

303.330US3

PATEN

Title:

ULTRA HIGH DENSITY FLASH MEMORY

### SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents P.O.Box 1450

Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants have included the fee of \$180.00 as set forth in 37 C.F.R. §1.17(p). Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

### Concise Explanations of Relevance

In accordance with 37 CFR 1.98(a)(3), Applicants submit, below, a concise explanation of relevance for the single, non-English reference. Further, Applicants submit additional general statements of relevance for the remaining U.S. Patents that are included on the attached 1449 Form, even though these general statements are not required.

03/04/2003 MBLANCO 00000019 09866938

01 FC:1805

180.00 DP

Foreign Patent Document

, ,	Document No	Name of Patentee or Applicant of cited Document	Concise Explanation of Relevance
JP-63-	I ID 63 066063   Minegighi K   I		Capacitor formed in lattice-like grooves in a semiconductor substrate

### **US Patent Documents**

USP Document Number	Name of Patentee or Applicant of cited Document	Concise Explanation of Relevance		
US-4,673,962	Chatterjee, et al.	Trench transistor.		
US-4,920,065	Chin, Daeje, et al.	Trench transistor.		
US-5,006,909	Kosa, Yasunobu	Semiconductor device with pillar-shaped portion.		
US-5,017,504	Nishimura, , et al.	Trench transistor.		

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Title: ULTRA HIGH DENSITY FLASH MEMORY

US-5,021,355	Dhong,, et al.	Trench transistor.
US-5,057,896	Gotou, H.	Semiconductor device with pillar-shaped portion.
US-5,072,269	Hieda, Katsuhiko	Semiconductor device with pillar-shaped portion.
US-5,177,576	Kimura, Shinichiro, et al.	Semiconductor device with pillar-shaped portion.
US-5,396,093	Lu, C.	Vertical DRAM cell.
US-5,414,287	Hong, G.	Semiconductor device with silicon islands.
US-5,432,739	Pein, Howard B.	Semiconductor device with pillar-shaped portion.
US-5,451,538	Fitch, J.T., et al.	Trench transistor.
US-5,460,988	Hong, Gary	Semiconductor device with silicon islands.
US-5,483,094	Sharma, U., et al.	Semiconductor device with pillar-shaped portion.
US-5,495,441	Hong, G.	Trench transistor.
US-5,519,236	Ozaki, Tohru	Semiconductor device with silicon columns.
US-5,563,083	Pein, Howard B.	Semiconductor device with pillar-shaped portion.
US-5,691,230	Forbes, L.	Semiconductor device with silicon islands.
US-5,874,760	Burns Jr., S. M., et al.	Semiconductor device with pillar-shaped portion.
US-5,879,971	Witek, K.	RAM cell with trench regions.
US-5,909,618	Forbes, L., et al.	Same inventive entity. Semiconductor device with pillar-shaped portion.
US-5,914,511	Noble, W. P., et al.	Same inventive entity. Semiconductor device with pillar-shaped portion.
US-5,933,717	Hause, Frederick N., et al.	Trench transistor.
US-5,943,267	Sekariapuram, S., et al.	Trench memory cell.
US-6,072,209	Noble, Wendell P., et al.	Same inventive entity. Semiconductor device with pillar-shaped portion.
US-6,172,391	Goebel, Bernd	Semiconductor structure with trenches.
US-6,208,164	Noble, W. P., et al.	Same inventive entity. Semiconductor device with pillar-shaped portion.

## Other Non-Patent Documents

Include name of the author (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Concise Explanation of Relevance 280
PEIN, H., et al., "A 3-D Sidewall Flash EPROM Cell and Memory Array", <u>IEEE Transactions on Electron Devices</u> , 40, (Nov. 1993),2126-2127	Semiconductor device with pillar-shaped portion.
PEIN, H., et al., "Performance of the 3-D PENCIL Flash EPROM Cell	Semiconductor device with pillar-shaped portion.

# SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT STATE OF THE PROPERTY OF THE PR

Include name of the author (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Concise Explanation of Relevance
and Memory Array", IEEE	
Transactions on Electron Devices,	
42, (November, 1995),1982-1991	
PEIN, H. B., et al., "Performance of	Semiconductor device with pillar-shaped portion.
the 3-D Sidewall Flash EPROM	
Cell", <u>IEEE International Electron</u>	
Devices Meeting, Technical Digest,	
(1993),11-14	
TAKATO, H., et al., "High	Semiconductor device with pillar-shaped portion.
Performance CMOS Surrounding	
Gate Transistor (SGT) for Ultra	
High Density LSIs", IEEE	
International Electron Devices	
Meeting, Technical Digest,	
(1988),222-225	

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AUG-5 2003

Serial No :09/866938 Filing Date: May 29, 2001 Title: ULTRA HIGH DENSITY FLASH MEMORY

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

WENDELL P. NOBLE JR. ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 31st day of July, 2003.

Signature

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
Puse as many sheets as necessary)

Application Number 09/866938

Filing Date May 29, 2001

First Named Inventor Noble Jr., Wendell

Group Art Unit 2813

Examiner Name Chen, Jack

Attorney Docket No: 303.330US3

Sheet 1 of 2

	LIOD D		ATENT DOCUMENT		Subclass	Filing Date
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	If Appropriate
	US-4,673,962	06/16/1987	Chatterjee, P. K., et al.	357	23.6	03/21/1985
	US-4,920,065	04/24/1990	Chin, Daeje , et al.	437	52	10/27/1989
	US-5,006,909	04/09/1991	Kosa, Yasunobu	357	23.6	10/30/1989
	US-5,017,504	05/21/1991	Nishimura, , et al.	437	40	04/21/1989
	US-5,021,355	06/04/1991	Dhong, , et al.	437	35	05/18/1990
	US-5,057,896	10/01/1991	Gotou, H.	357	49	05/30/1989
	US-5,072,269	12/10/1991	Hieda, Katsuhiko	357	23.6	03/15/1989
	US-5,177,576	01/05/1993	Kimura, Shinichiro, et al.	257	71	05/06/1991
	US-5,396,093	03/07/1995	Lu, C.	257	306	08/12/1994
	US-5,414,287	05/09/1995	Hong, G.	257	316	04/25/1994
- "	US-5,432,739	07/11/1995	Pein, Howard B.	365	185	06/17/1994
	US-5,451,538	09/19/1995	Fitch, J.T., et al.	487	60	04/20/1994
	US-5,460,988	10/24/1995	Hong, Gary	437	43	04/25/1994
	US-5,483,094	01/09/1996	Sharma, U., et al.	257	316	09/26/1994
	US-5,495,441	02/27/1996	Hong, G.	365	185.01	05/18/1994
	US-5,519,236	05/21/1996	Ozaki, Tohru	257	302	06/27/1994
	US-5,563,083	10/08/1996	Pein, Howard B.	437	43	04/21/1995
	US-5,691,230	11/25/1997	Forbes, L.	437	62	09/04/1996
	US-5,874,760	02/23/1999	Burns Jr., S. M., et al.	257	315	01/22/1997
	US-5,879,971	03/09/1999	Witek, K.	438	238	09/28/1995
	US-5,909,618	06/01/1999	Forbes, L., et al.	438	242	07/08/1997
	US-5,914,511	06/22/1999	Noble, W. P., et al.	257	302	10/06/1997
	US-5,933,717	08/03/1999	Hause, Frederick N., et al.	438	200	03/04/1997
	US-5,943,267	08/24/1999	Sekariapuram, S., et al.	365	185.28	06/12/1998
<del></del>	US-6,072,209	06/06/2000	Noble, Wendell P., et al.	257	296	07/08/1997
	US-6,172,391	01/09/2001	Goebel, Bernd	257	305	08/27/1998
	US-6,208,164	03/27/2001	Noble, W. P., et al.	326	41	08/04/1998

**EXAMINER** 

**DATE CONSIDERED** 

PTO/SB/08A(10-01)
Approved for use through 10/31/2002, 2008 651-0031
US Patent & Trademark Office. U.S. DEPARTMENT OF COMMERCE
the Paperwork Reduction Act of 1996, no persons are required to respond to a collection of information unless it contains a valid OMB control number. Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE 09/866938 Applicati n Number STATEMENT BY APPLICANT 1956 as many sheets as necessary) May 29, 2001 Filing Date Noble Jr., Wendell **First Named Inventor Group Art Unit** 2813 Chen, Jack **Examiner Name** Attorney Docket No: 303.330US3 Sheet 2 of 2

FOREIGN PATENT DOCUMENTS						
Examiner Foreign Document No Initials*		Publication Date Name of Patentee or Applicant of cited Document		Class	Subclass	T²
	JP-63-066963	03/25/1988	Minegishi, K.	HO1 L	27/10	

		R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	T =2
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	,-
		PEIN, H., et al., "A 3-D Sidewall Flash EPROM Cell and Memory Array", IEEE	
		Transactions on Electron Devices, 40, (Nov. 1993),2126-2127	
		PEIN, H., et al., "Performance of the 3-D PENCIL Flash EPROM Cell and	
		Memory Array", IEEE Transactions on Electron Devices, 42, (November,	
		1995),1982-1991	
	_	PEIN, H. B., et al., "Performance of the 3-D Sidewall Flash EPROM Cell", IEEE	
		International Electron Devices Meeting, Technical Digest, (1993),11-14	
	- <del></del>	TAKATO, H., et al., "High Performance CMOS Surrounding Gate Transistor	Γ
	!	(SGT) for Ultra High Density LSIs", IEEE International Electron Devices Meeting,	
		Technical Digest, (1988),222-225	

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Jack Chen

Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

AUG 0 4 2003 E

Serial No.: 09/866938

Due Date: N/A

Group Art Unit: 2813

We are transmitting herewith the following attached items (as indicated with an "X"):

 $\underline{X}$  A return postcard.

- $\overline{\underline{X}}$  An Supplemental Information Disclosure Statement (4 pgs.), Form 1449 (2 pgs.), and copies of 32 cited documents
- $\underline{X}$  A check in the amount of \$180.00 to cover the fee for consideration of Information Disclosure Statement under 97(c).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

Atty: Daniel J. Kluth

<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this <u>31st</u> day of July, 2003.

Name

Signature

**Customer Number 21186** 

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